CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A PCRAM device, comprising:

a first and second digit line;

first and second programmable conductor memory elements for storing complementary binary digit values;

first and second access devices for respectively coupling said first and second conductor memory elements to said first and second digit lines; and

a sense amplifier having inputs respectively coupled to said first and second digit lines for reading a binary value stored as a resistance value in one of said memory elements.

2. A device as in claim 1 further comprising a precharge circuit for precharging said digit lines to a common precharge voltage prior to a read operation.

3. A device as in claim 1 further comprising a pair of row lines respectively coupled to said first and second access devices; and

circuitry for simultaneously activating said first and second row lines and therefore activating said first and second access devices.

4. A device as in claim 3 wherein said first and second access devices are access transistors.

5. A device as in claim 1 wherein said first and second programmable conductor memory elements are formed of a chalcogenite glass.

6. A device as in claim 3 wherein when said access devices are activated, said precharge voltage on said digit lines discharges through a respective resistance of said first and second programmable conductor memory devices, said sense amplifier determining which of said memory devices has a high and low resistance state and outputting a binary value corresponding to the resistance state of said one memory element.

7. A device as in claim 2 wherein said digit lines have an associated parasitic capacitance which stores said precharge voltage.

8. A device as in claim 2 wherein said parasitic capacitance stores a voltage value which is larger than said precharge voltage.

9. A device as in claim 3 wherein said row lines are activated in a manner which prevents an automatic refresh of at least one of said memory elements during a read operation.

10. A device as in claim 3 wherein said row lines are activated in a manner which causes an automatic refresh of at least one of said memory elements during a read operation.

11. A device as in claim 1 wherein said first and second memory elements are in a common memory array.

12. A device as in claim 1 wherein said first and second memory elements are in different memory arrays.

13. A device as in claim 2 further comprising an equilibrate circuit for equilibrating the voltage on said digit lines.

14. A memory device comprising:

a plurality of pairs of first and second programmable conductor random access memory cells, each pair of memory cells comprising:

first and second programmable conductor memory elements for storing complementary binary digit values;

first and second access devices for respectively coupling said first and second conductor memory elements to first and second digit lines; and

a sense amplifier having inputs respectively coupled to said first and second digit lines for reading a binary value stored as a resistance value in one of said memory elements.

15. A device as in claim 14 further comprising a precharge circuit for precharging said digit lines to a common precharge voltage prior to a read operation.

16. A device as in claim 14 further comprising a pair of row lines respectively coupled to said first and second access devices; and

circuitry for simultaneously activating said first and second row lines and therefore activating said first and second access devices.

17. A device as in claim 16 wherein said first and second access devices are access transistors.

18. A device as in claim 14 wherein said first and second programmable conductor memory elements are formed of a chalcogenite glass.

19. A device as in claim 16 wherein when said access devices are activated, said precharge voltage on said digit lines discharges through a respective resistance of said first and second programmable conductor memory devices, said sense amplifier determining which of said memory devices has a high and low resistance state and outputting a binary value corresponding to the resistance state of said one memory element.

20. A device as in claim 15 wherein said digit lines have an associated parasitic capacitance which stores said precharge voltage.

21. A device as in claim 15 wherein said parasitic capacitance stores a voltage value which is larger than said precharge voltage.

22. A device as in claim 16 wherein said row lines are activated in a manner which prevents an automatic refresh of at least one of said memory elements during a read operation.

23. A device as in claim 16 wherein said row lines are activated in a manner which causes an automatic refresh of at least one of said memory elements during a read operation.

24. A device as in claim 14 wherein said first and second memory elements are in a common memory array.

25. A device as in claim 14 wherein said first and second memory elements are in different memory arrays.

26. A device as in claim 15 further comprising an equilibrate circuit for equilibrating the precharge voltage on said digit lines.

27. A device as in claim 14 wherein said memory device is provided on a memory module.

28. A device as in claim 27 wherein said memory module is a plug-in memory module.

29. A computer system comprising:

a processor;

a memory system coupled to said processor, said memory system comprising:

a first and second digit line;

first and second programmable conductor memory elements for storing complementary binary digit values;

first and second access devices for respectively coupling said first and second conductor memory elements to said first and second digit lines; and

a sense amplifier having inputs respectively coupled to said first and second digit lines for reading a binary value stored as a resistance value in one of said memory elements.

30. A system as in claim 29 further comprising a precharge circuit for precharging said digit lines to a common precharge voltage prior to a read operation.

31. A system as in claim 29 further comprising a pair of row lines respectively coupled to said first and second access devices; and

circuitry for simultaneously activating said first and second row lines and therefore activating said first and second access devices.

32. A system as in claim 31 wherein said first and second access devices are access transistors.

33. A system as in claim 29 wherein said first and second programmable conductor memory elements are formed of a chalcogenite glass.

34. A system as in claim 31 wherein when said access devices are activated, said precharge voltage on said digit lines discharges through a respective resistance of said first and second programmable conductor memory devices, said sense amplifier determining which of said memory devices has a high and low resistance state and outputting a binary value corresponding to the resistance state of said one memory element.

35. A system as in claim 30 wherein said digit lines have an associated parasitic capacitance which stores said precharge voltage.

36. A system as in claim 30 wherein said parasitic capacitance stores a voltage value which is larger than said precharge voltage.

37. A system as in claim 31 wherein said row lines are activated in a manner which prevents an automatic refresh of at least one of said memory elements during a read operation.

38. A system as in claim 31 wherein said row lines are activated in a manner which causes an automatic refresh of at least one of said memory elements during a read operation.

39. A system as in claim 29 wherein said first and second memory elements are in a common memory array.

40. A system as in claim 29 wherein said first and second memory elements are in different memory arrays.

41. A system as in claim 30 further comprising an equilibrate circuit for equilibrating the voltage on said digit lines.

42. A method of operating a programmable conductor memory device comprising:

storing a binary value as respective different resistance states in a first and second programmable conductor memory element;

determining a binary value stored in one of said memory elements by discharging respective voltages through said memory elements and comparing the discharging voltages.

43. A method as in claim 42 wherein said discharging comprises:

precharging complementary digit lines to a voltage value; and

discharging the voltage value on each of said complementary digit lines through a respective memory element.

44. A method as in claim 43 wherein said precharged voltage value on said complementary digit lines is discharged through said respective memory elements by enabling access transistors respectively associated with each of said memory elements.

45. A method as n claim 44 further comprising completing said precharge before enabling said access transistors.

46. A method as in claim 45 further comprising equilibrating said digit lines before enabling said access transistors.

47. A method as in claim 44 where said comparison comprises:

determining whether the discharging voltage associated with one memory element is the higher or lower of the two discharging voltages and outputting a first binary value if the discharging voltage associated with the said one memory element is the higher voltage and outputting a second binary value if the discharging voltage associated with said one memory element is the lower voltage.

48. A method as in claim 47 further comprising setting a digit line having a higher discharge voltage to a first predetermined voltage state and setting a digit line having a lower discharging voltage to a second predetermined voltage state.

49. A method as in claim 48 wherein said first predetermined voltage is higher than said second predetermined voltage.

50. A method as in claim 49 wherein said second predetermined voltage is ground voltage.

51. A method as in claim 48 further comprising disabling said access transistors before said digit lines are set to said first and second voltage states.

52. A method as in claim 48 further comprising enabling at least one of said access transistors during a time when said digit lines are set to said first and second voltage states.

53. A method of producing a programmable conductor memory device, said method comprising;

forming first and second digit lines;

forming first and second programmable conductor memory elements;

forming first and second access transistors for respectively coupling said first and second memory elements to said first and second digit lines;

forming a precharge circuit for precharging said first and second digit lines to a first voltage;

forming respective row lines for operating said access transistors to couple said memory elements to respective digit lines; and

forming a sense amplifier which has inputs respectively coupled to said digit lines.

54. A method as in claim 53 further comprising forming a row decoder for decoding row address signals and selectively and simultaneously enabling said word lines.

55. A method as in claim 53 wherein said memory elements are formed of a chalcogenite glass.

56. A method as in claim 53 wherein said memory elements are fabricated in a common memory array.

57. A method as in claim 53 wherein said memory elements are fabricated in different memory arrays.

58. A method as in claim 53 further comprising forming an equilibrate circuit for equilibrating said digit lines.